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10/026,880	12/27/2001	Ryuichi Hata	111468	9980

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,880	HATA, RYUICHI	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 17-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 17-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 7.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 17, 21, 31, 32, and 34 are objected to because of the following informalities:

On line 7, of Claim 17, the phrase "arranged outside each memory blocks" should be "arranged outside each of the memory blocks". Appropriate correction is required.

On line 6, of Claim 21, "each stores the data..." should be "each circuit storing data..."

On line 4, of Claim 31, "each stores the data..." should be ", each circuit storing data..."

On line 5, of Claim 32, "physical segment is search" should be "physical segment is the search".

On line 2, 3, and 4 respectively, of Claim 34, converting circuit output" should be "converting circuit outputs"; "and physical segment" should be "and the physical segment"; "executes search operation" should be "executes the search operation".

Specification

2. The amendment filed on March 3rd, 2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

On Page 6, paragraph 27, the change of "number" to "position or location" is not supported by the original disclosure. A number (as originally disclosed) is not the same as a position or location; a position or location is the same as an address; which is never referred to as a number.

On Page 7, paragraph 29, line 2, the change of "which search" to "to be searched" is not supported by the original disclosure. As originally disclosed, the specification described, "circuits which search", thus implying that the circuits performed the search. As amended, the specification discloses "circuits to be searched", describing the search being conducted by another component which is searching in the circuits. These teachings are opposites.

Support for the amendments presented must be present in the specification as originally filed.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 17, 21, 22, 30, and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claims 17 and 30, when read in context, is it is not clear what "maximum number of combinable words" refers to.

Regarding Claims 21 and 31, it is not understood what "and which are searched for a match" refers to. It is unclear as to what is being searched.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 17-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al. (6,553,453) in view of Kanazawa et al. (6,611,445).

Regarding Claims 17 and 30, Gibson et al. discloses a content addressable memory having a function for extending a data width, comprising:

a plurality of memory blocks ("CAM blocks") each having a plurality of CAM words, the plurality of memory blocks are divided into the same number of physical segments as maximum number of combinable words to form an entry ("configured to store a plurality of variable widths... one or more data portions, Column 2, lines 59-67);

entry configuration set means for setting the number of CAM words which are combined to form an entry ("tags encode the widths", Column 5, lines 35-39 and Column 3, lines 20-27);

and a logical-segment-to-be-searched signal indicating a position of words to be searched ("search_data", Figure 2B).

The entry configuration set means of Gibson et al. is arranged outside each memory block since it is provided by an external component ("outside the memory block") and it is placed in a separate field 276a, outside the memory block 276b (Figure 2B)

Gibson et al. does not teach a logical-segment-to-physical-segment converting circuit. However, Gibson does implicitly disclose logical to physical conversion since logical search data is used to form an indication of the location of the words being searched.

Kanazawa et al. discloses a logical-segment-to-physical-segment converting circuit 66 for converting logical-segment-to-be-searched signal that indicates a position of words to be

searched to the physical-segment-to-be-searched instruction signal according to the setting of said entry configuration set means (Column 2, lines 1-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the logical-to-physical converting circuit of Kanazawa to the system of Gibson et al. since such a converting circuit would enable the logical to physical conversion of Gibson et al. and since the converting circuit is a dedicated circuit, it would prevent formatting conflicts in the system, thus reducing errors and delays.

Regarding Claims 21 and 31, Gibson et al. discloses a content addressable memory wherein the physical segments each comprise:

a search bit line ("CAM blocks receiving search data portions", Figure 2B, 276b);

a search bit line divider for dividing the search bit line according to search data (Figure 2B, 282a acts as physical divider); and

a plurality of one-word circuits, each storing the data of one word; which are searched for a match between the stored data and the search data driven on the search bit line to output a search result ("encoders configured for concatenating the specified number of CAM blocks to generate one or more search results", Column 3, lines 1-15). A data driver to drive search data portions to the CAM blocks must be present for the operation of the system.

Regarding Claims 18 and 22, Gibson et al. discloses a content addressable memory wherein said entry configuration set means is capable of setting the number of words which is a divisor of the maximum number of words which are combined, where the divisor includes 1 and the maximum number of words which are combined ("tags encode the widths from 32-bits to 256-bits", Column 5, lines 35-39).

Regarding Claims 19, 23, and 28, Gibson et al. discloses a content addressable memory according to claim 18, wherein said entry configuration set means is a register (Figure 2B, 276a).

Regarding Claims 20, 24, and 29, Gibson et al. discloses a content addressable memory wherein the register is a register having a bit width corresponding to the number of said physical segments (Figure 2B, 276a and "2-bit tag encode variable data widths", Column 5, lines 35-39).

Regarding Claim 25, Gibson et al. discloses a content addressable memory wherein each of the one-word circuits (CAM blocks) includes a CAM word having a plurality of CAM cells ("configured to store a plurality of variable widths... one or more data portions, Column 2, lines 59-67), and word logic for processing the search result output from the CAM word (Figure 2B, 260); the word logic includes a match flag register for holding the search result ("Search_Result"), and AND chain for processing the match flag data of the plurality of words coupled to each other in an entry; and an entry match output circuit for outputting a match flag for the entry (260).

Regarding Claim 26, Gibson et al. discloses a content addressable memory each of the physical segments (270, 272, 274, Figure 2B) further including a match flag control signal generating circuit for generating a match flag control signal which is a timing signal for capturing and holding the search result output from the one-word circuit (262).

Regarding Claim 27, Gibson et al. disclose a content addressable memory wherein when a search operation is executed; only the search bit line in a physical segment to be searched ("Search_data") is driven by the search bit line driver. A data driver to drive search data portions to the CAM blocks must be present for the operation of the system. .

Regarding Claim 32, Gibson et al. discloses a content addressable memory wherein, said entry configuration set means (Tag 276a) outputs entry representative physical segment instruction signal (Search_Data signal) to each physical segment according to the setting of the entry configuration (276a)), and after search operation for one or more words within an entry is executed, search result output from the one-word circuit in the representative physical segment is search result of the entry (search result from Encoder 262).

Regarding 33, Gibson et al. discloses a content addressable memory, the word having the smallest address or the largest address within an entry is designated as representative word of the entry. Any word in the system can be considered a representative word since any can be of the smallest or largest address.

Regarding Claim 34, Gibson et al. discloses a content addressable memory. Gibson does not disclose a logical-segment-to-physical segment converting circuit. Kanazawa et al. discloses a logical-segment-to-physical-segment converting circuit for converting logical-segment-to-be-searched signal that indicates a position of words to be searched to the physical-segment-to-be-searched instruction signal according to the setting of said entry configuration set means (Column 2, lines 1-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the logical-to-physical converter of Kanazawa to the system of Gibson et al. since such a converter could prevent formatting conflicts in the system, thus reducing errors and delays. In combining the invention of Kanazawa with the system of Gibson et al., the converting circuit would output physical segment to be searched instruction signal to each physical segment, and physical segment instructed to search would be used for the search operation.

Regarding Claim 35, Gibson et al. discloses a content addressable memory, wherein each of the one-word circuits includes a CAM word having a plurality of CAM cells ("CAM blocks configured to store a plurality of variable widths... one or more data portions, Column 2, lines 59-67), and word logic for processing the search result output from the CAM word (Figure 2B); the word logic further includes: a match flag register for holding the search result (262); an AND chain for processing the match flag data of the plurality of words coupled to each other in an entry; and an entry match output circuit for outputting a match flag for the entry (260).

Regarding Claim 36, Gibson et al. discloses a content addressable memory wherein the CAM cells are mismatch-detection type CAM cells. The CAM cells can be considered mismatch detection cells since a comparison is being made in the search operation and a match/mismatch is what determines the results of the search.

Response to Arguments

7. Applicant's arguments filed on March 3rd, 2004 have been fully considered but they are not persuasive.

Applicant argues that the logical-segment-to-physical segment of Kanazawa et al. (Naoki) does not indicate the position of words to be searched. The logical to physical converter of Kanazawa et al. teaches the conversion of CAM word addresses, since CAM word addresses designate the position of words; the logical-segment-to-physical segment of Kanazawa et al. (Naoki) indicates the position of words to be searched.

Applicant tries to distinguish a logical segment as an index that indicates a word position. However, this can also be the description of a logical address or any location identifier (user

word addresses). Applicant also defines a physical segment as a physical memory block, yet this concept can also be construed as a physical address (inner word addresses).

Applicant also tries to distinguish from the invention of Gibson et al. by stating that the entry configuration set means is outside of the memory block. However, being that the tag area is separate from the search data area (See Figure 2B of Gibson) this can be construed as "outside the memory block"). Additionally, since the Tag value is being provided to the CAM from an outside source, this can too be interpreted as "placed outside the memory block".

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
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